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Modified SPWM Based Level Saturated PWM Strategy to Reduce the Switching Loss and THD of 5-Level NPC Inverters

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Abstract— Neutral-point-clamped (NPC) multilevel inverters (MLIs) are becoming popular for medium to high power applications. It has some major performance criteria such as the total harmonic distortion (THD) of the output line voltage and grid current, power losses, inverter efficiency etc. which are greatly influenced by the pulse width modulation (PWM) strategy. In order to improve the performance and reduce the switching losses, a sinusoidal PWM (SPWM) based level saturated PWM strategy is suggested in this work. For the comparative analysis, a five level three phase grid-tied NPC inverter topology is considered. The saturated region of the proposed PWM technique can significantly reduce the THD of the output line voltage and grid current as well as the switching losses. To prove the superiority of the proposed PWM strategy, it is compared with the other existing PWM techniques in terms of THD of the output line voltage, grid current and power loss. The simulation part of the whole system is conducted in MATLAB Simulink as well as PLECS simulation platform.

Index Terms— Neutral point clamped, multilevel inverter, total harmonic distortion, pulse width modulation, SPWM, saturated region, switching losses.

1 Introduction

MULTILEVEL inverters are widely adopted topology in the field of medium to high power applications as it offers some benefits such as lower harmonic content than the two-level voltage source inverter, lower filter size etc. Neutral point clamped inverter is a popular variant among multilevel inverter topologies because of its higher effectiveness, simplicity, lower components etc. [1]. However, there are some parameters which affect the overall performance of these inverters such as harmonic distortion of the output line voltage and grid current, switching and conduction losses, efficiency etc. These performance parameters can be controlled by the applied pulse width modulation techniques [2].

In the field of power applications, power efficiency is a crucial challenging fact as it is directly corelated with the power loss of the inverter. The reduction in power loss indicates the higher effectiveness of the inverter. The switching losses and conduction losses of the power IGBTs and diodes are typically the sources of power losses in multilevel inverters [3]. Based on the switching instants of the PWM techniques, switching losses are occurred. Therefore, lowering the switching losses through a significant reduction in switching instants can also lower the switching of the power IGBTs and diodes. An effective PWM technique that is widely used to mitigate switching losses is discontinuous pulse width modulation (DPWM). A direct digital technique that utilizes a general DPWM (DDT- GDPWM) is presented in [4] for reducing the switching losses. A real time optimization strategy is reported in [5] which reduces the switching losses of the 3L-NPC inverter. But the THD of the grid current is higher and optimization method is relatively complex in the proposed strategy.

There are some existing PWM techniques which are widely used to control the performance parameters of the multilevel inverters. In [6], sinusoidal PWM (SPWM) technique is applied in the nested T-type NPC inverter which offers higher output line voltage THD and switching losses. A virtual space vector PWM (SVPWM) and third harmonic injected PWM (THPWM) have been developed for the NPC inverter in [7]-[8], respectively. These PWM techniques offer some specific improvements in the power quality but have considerably higher harmonic distortion and switching losses. On the contrary, bus clamping PWM (BCPWM) has a great ability to reduce the THD and the power losses of the inverter at a same time. In [9], a reference saturated third harmonic injected equal loading PWM is proposed to minimize the harmonic distortion of the output line voltage and power loss of voltage source inverter. To reduce the switching losses, third harmonic injected sixty-degree BCPWM (THSDBCPWM) and the third harmonic injected TDBCPWM (THTDBCPWM) techniques are applied in medium voltage grid-tied converter in [10].

Recently, carrier based PWM techniques are gaining popularity in field of medium to high power application [11]. Some common carrier based PWM techniques are phase disposition PWM (PDPWM), phase opposite disposition PWM (POD-PWM), alternate phase opposite disposition PWM (APOD-PWM), interleaved carrier PWM (ICPWM) etc. which have been analyzed and compared using NPC inverter in [12].

In this work, a sinusoidal PWM (SPWM) based level saturated PWM technique is proposed considering the aforementioned power quality concerns. The proposed PWM offers the following advantages over the other existing PWM techniques:

- Mitigates the harmonic distortion of the output line

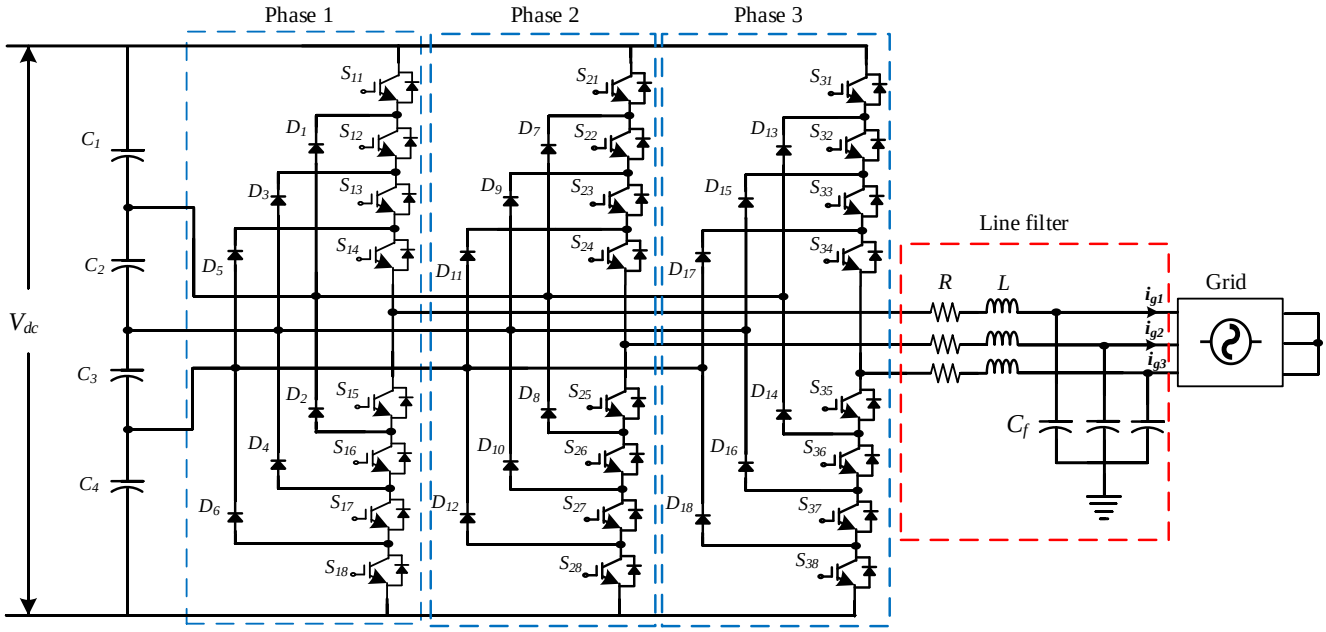

Fig. 1. Circuit diagram of a grid-tied three phase five-level NPC inverter.

voltage and grid current of the inverter.

- Reduces the switching losses and conduction losses of the inverter.
- Doesn't need any optimization or other strategy which means it is simple and easy to develop.

2 Inverter Topology

Fig. 1 depicts the basic circuit diagram of a grid-tied three phase five level NPC inverter. At the input side, four dc-link capacitors (C_1, C_2, C_3 and C_4) are used to divide the DC voltage (V_{dc}). To generate the five-level output, each phase required total eight insulated-gate bipolar transistors (IGBTs) that are (S_{11}, S_{12}, S_{13}, S_{14}, S_{15}, S_{16}, S_{17}, S_{18}) respectively. Thus, for three phase output total twenty-four IGBTs are required. At the output side, line filter is connected before connecting to the grid in order to mitigate the harmonics from the inverter output.

3 The Existing PWM Techniques

Among the PWM techniques, most common and widely used PWM techniques are sinusoidal PWM (SPWM), conventional space vector PWM (CSVPWM), third harmonic injected PWM (THPWM). SPWM is the simplest PWM technique for the MLIs. But the performance indices in this technique are poor as compared to other PWM techniques. It offers higher harmonic distortion which is the major drawback in grid tied applications. Moreover, it has higher switching loss than other techniques. On the contrary, the CSVPWM and THPWM are better than the SPWM technique. They offer lower harmonic distortion and switching losses which is desirable for the MLIs. However, the harmonic distortion and the switching losses can be further improved by the proposed PWM technique. The reference signals of the well-known existing PWM techniques and the proposed techniques are depicted in Fig. 2.

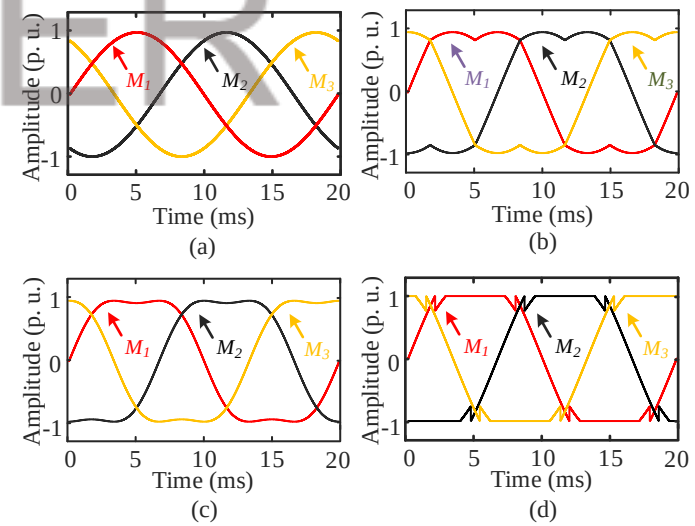

Fig. 2. Reference signal of different PWM techniques (a) SPWM (b) CSVPWM (c) THPWM and (d) the proposed PWM.

4 The Proposed PWM Technique

The block diagram representation of the generation procedure of the proposed PWM technique is depicted in Fig. 3. The proposed PWM technique is generated by modifying the SPWM signal. At first, a three-phase sinusoidal signal is taken such

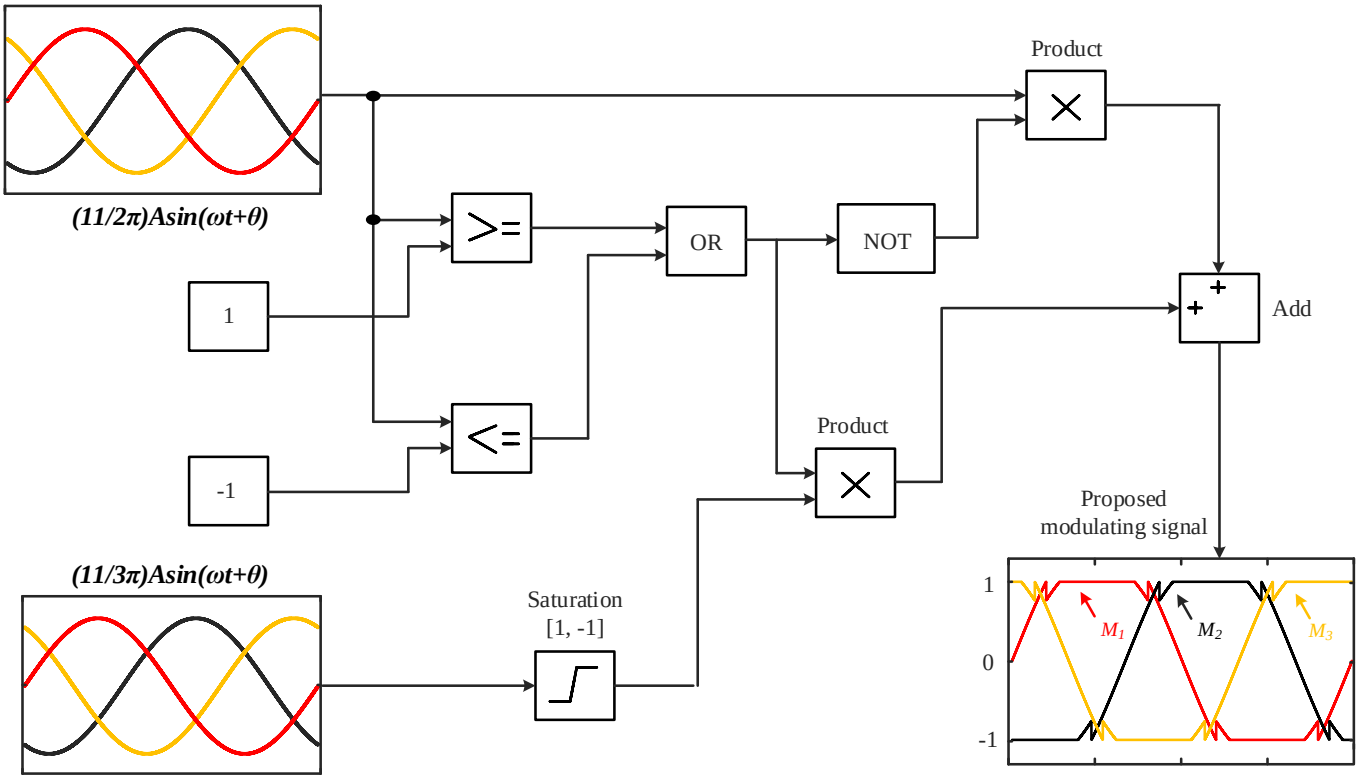

Fig. 3. Generation procedure of the proposed PWM technique.

that:

$$X = \frac{11}{2\pi}[A\sin(\omega t + \theta) \tag{1}$$

$$\lfloor X_1 \quad X_2 \quad X_3 \rfloor = \lfloor X_{\theta=0^\circ} \quad X_{\theta=-120^\circ} \quad X_{\theta=120^\circ} \rfloor \tag{2}$$

where, A is the amplitude and ω is the angular frequency of the signal, respectively. Then, the signal X is compared with 1 and -1 to generate the pulse signal M and N, respectively such that:

$$M = \begin{cases} 1 & ;if\ X \geq 1 \\ 0 & ;otherwise \end{cases} \tag{3}$$

$$N = \begin{cases} 1 & ;if\ X \leq -1 \\ 0 & ;otherwise \end{cases} \tag{4}$$

After that, another pulse signals O and P are constructed by using the previously generated pulse signals M and N that is expressed as follows:

$$P = \overline{O} = \overline{M + N} \tag{5}$$

Now, another three-phase sinusoidal signal is taken such that:

$$Y = \frac{11}{3\pi}[A\sin(\omega t + \theta) \tag{6}$$

$$\lfloor Y_1 \quad Y_2 \quad Y_3 \rfloor = \lfloor Y_{\theta=0^\circ} \quad Y_{\theta=-120^\circ} \quad Y_{\theta=120^\circ} \rfloor \tag{7}$$

Then, another signal Z is generated using saturation by the limit [1, -1]. At last, the final modulating signal is developed by multiplication and division operation with the previously generated signals that is expressed as follows:

$$M = OZ + PX \tag{8}$$

$$\lfloor M_1 \quad M_2 \quad M_3 \rfloor = \lfloor M_{\theta=0^\circ} \quad M_{\theta=-120^\circ} \quad M_{\theta=120^\circ} \rfloor \tag{9}$$

Now. the generated modulating signal is compared with the carrier signal to generate the gate pulses for the power switches.

TABLE 1
PARAMETERS USED FOR CASE STUDY

Parameter	Simulation value
DC voltage, V_{dc}	500 V
Grid frequency, f_g	50 Hz
Grid current, i_g	230 V (rms)
Carrier frequency, f_c	2 kHz
Modulation index, m	1
DC-link capacitor (C_1, C_2, C_3, C_4)	5000 uF
IGBT module	IKW50N65F5
Body diode	IKW50N65F5
Line filter (R, L, C_f)	0.5 Ω, 8.5 mH, 100 uF

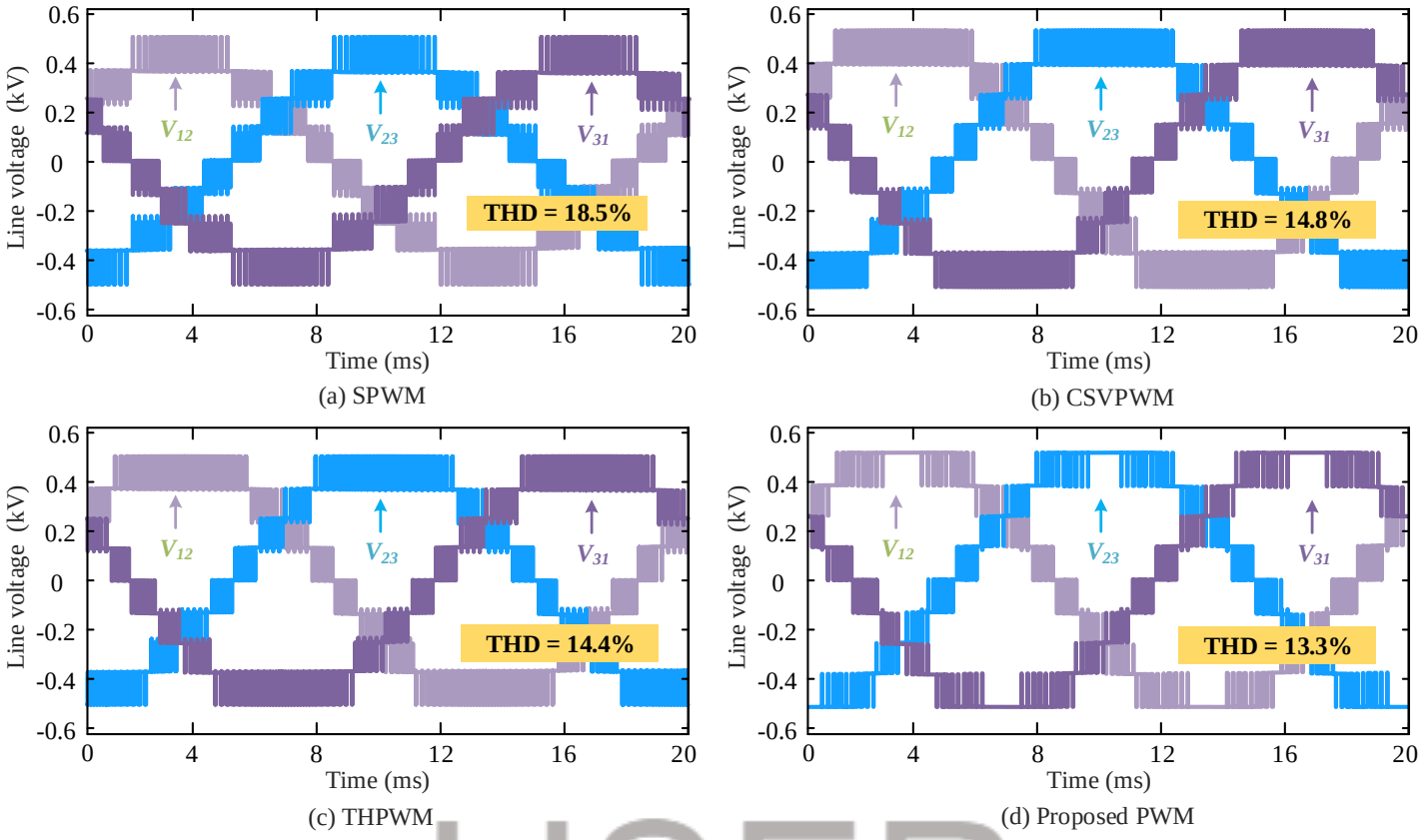

Fig. 4. Three phase unfiltered output line voltage of the inverter under different PWM techniques (a) SPWM (b) CSVPWM (c) THPWM and (d) the proposed PWM.

5 Performance Analysis

The comparative performance analysis between the SPWM, CSVPWM, THPWM and the proposed PWM techniques are conducted in MATLAB Simulink software with the parameters as given in Table I.

5.1 THD Analysis

Fig. 4 illustrates the three-phase unfiltered line voltage of the inverter under SPWM, CSVPWM, THPWM and the proposed PWM technique, respectively. The SPWM technique gives the highest output line voltage THD which is 18.5%. It is the major drawback using this technique because higher harmonic distortion is undesirable in grid-tied applications. The output line voltage THD obtained by the CSVPWM, THPWM and the proposed PWM techniques are 14.8%, 14.4% and 13.3%, respectively. The proposed PWM gives the lowest THD among other PWM techniques. Because of the clamping region of the modulating signal, the proposed PWM technique can significantly reduce the switching region resulting reduced output line voltage THD.

The three-phase grid current of the inverter using different PWM techniques are depicted in Fig. 5. The inverter output is filtered by a RLC line filter according to the values given in Table I. The grid current harmonics can be further reduced by designing a better line filter. From Fig. 5, it can be seen that SPWM. CSVPWM, THPWM and the proposed PWM gives 1.07%, 1.03%, 1.01% and 0.91% grid current THD, respectively. In this case, the proposed PWM technique gives the lowest grid current THD among the other existing techniques. The comparative overview between SPWM, CSVPWM, THPWM and the proposed PWM technique in terms of THD is given in Table II.

TABLE 2
Comparative THD Analysis Between Different PWM Techniques

PWM technique	Line voltage THD % (unfiltered)	Grid current THD % (filtered)
SPWM	18.5	1.07
CSVPWM	14.8	1.03
THPWM	14.4	1.01
Proposed PWM	13.3	0.91

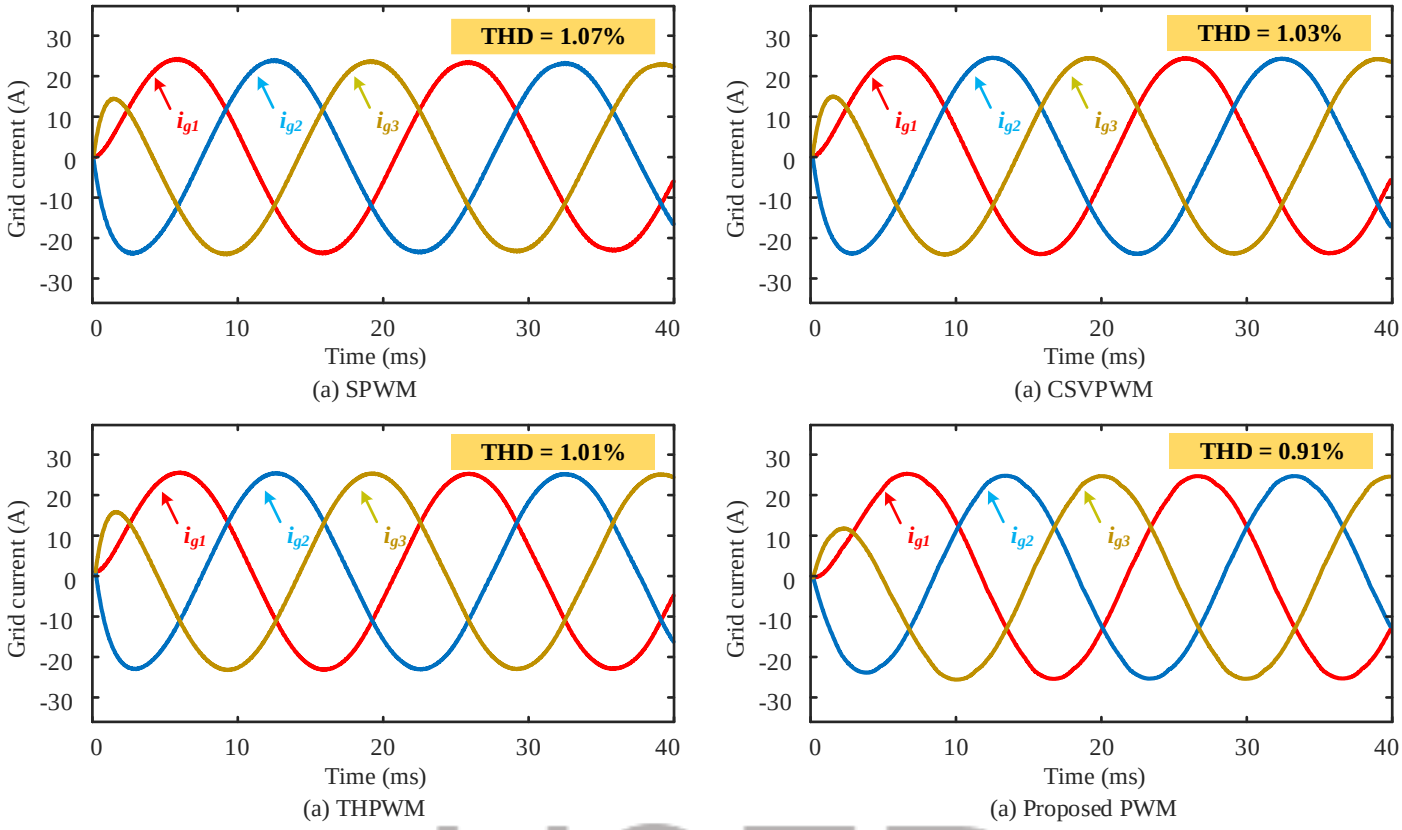

Fig. 5. Three phase grid current of the inverter under different PWM techniques (a) SPWM (b) CSVPWM (c) THPWM and (d) the proposed PWM.

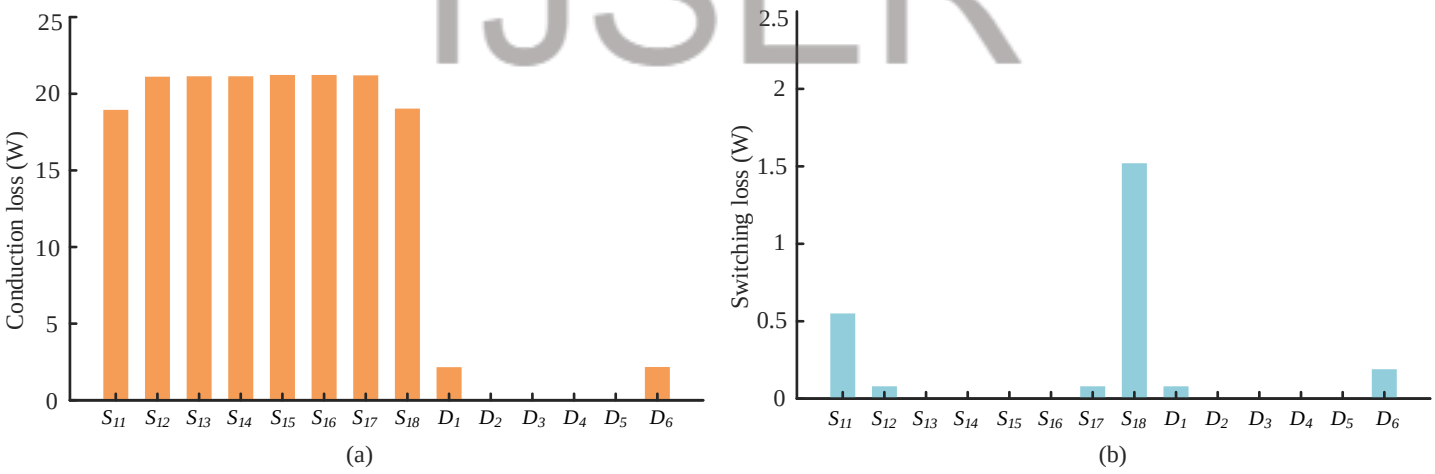

Fig. 6. Loss distribution among the power switches and diodes of a single phase under the proposed PWM technique (a) conduction loss and (b) switching loss.

5.1 Power Loss Analysis

The conduction loss and the switching loss distribution for a single phase under the proposed PWM technique are illustrated in Fig. 6(a) and 6(b), respectively. For calculating the power loss of the IGBTs PLECS simulation software is used. From the Infineon Technologies, IKW50N65F5 IGBT is selected and the characteristic curve of the model is placed in the PLECS block set to obtain the power losses. The comparative power loss analysis between the SPWM, CSVPWM, THPWM and the proposed PWM techniques are depicted in Fig. 7 and Table III for unity modulation index. The SPWM technique gives 4.16 W and 171.45 W switching loss and conduction loss, respectively. Similarly, 3.28 W and 3.31 W switching loss, 169.91 W and 170.21 W conduction loss is obtained under the CSVPWM and THPWM, respectively. However, the proposed PWM technique gives 2.73 W switching loss and 168.67 W conduction loss which is the lowest among other PWM techniques. Moreover, the proposed PWM technique offers 34.38%, 16.77% and 17.52% improved switching losses than

the existing SPWM, CSVPWM and THPWM, respectively. The improvement in power loss ensures that the efficiency of the inverter is higher under the proposed PWM technique. Thus, the proposed PWM is better than the other existing SPWM, CSVPWM and THPWM techniques.

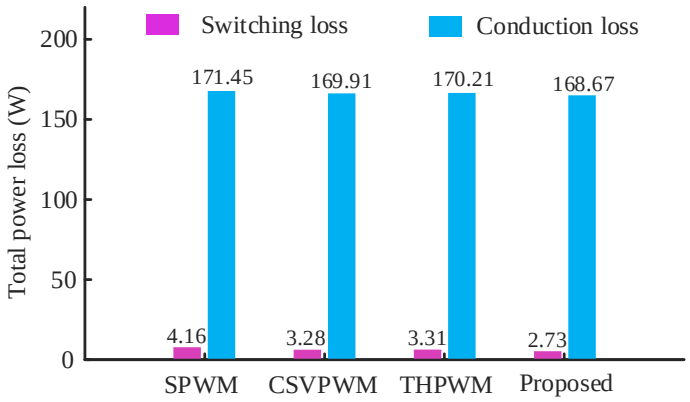

Fig. 7. Total power loss comparison among different PWM techniques for unity modulation index.

TABLE 3
COMPARATIVE POWER LOSS ANALYSIS BETWEEN DIFFERENT PWM TECHNIQUES

PWM technique	Switching loss (W)	Conduction loss (W)
SPWM	4.16	171.45
CSVPWM	3.28	169.91
THPWM	3.31	170.21
Proposed PWM	2.73	168.67

6 CONCLUSION

This work presents a SPWM based level saturated PWM technique utilizing a five-level grid-tied NPC inverter to mitigate the harmonic distortion of the inverter line voltage and grid current. The proposed PWM technique also reduces the switching and conduction losses of the inverter. The proposed PWM offers 13.3% output line voltage THD and 0.91% grid current THD which are lower than the existing SPWM, CSVPWM and THPWM, respectively. Moreover, the proposed PWM gives 2.71 W switching loss and 168.67 W conduction loss for unity modulation index which are also lower than the existing SPWM, CSVPWM and THPWM techniques, respectively. The reduction in both switching and conduction losses will increase the efficiency of the inverter. So, the proposed PWM technique can be considered as a smart choice in order to mitigate the harmonic distortion and reduce the switching losses of the NPC inverters for grid-tied applications.

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